88 - ACR

AUDIO CASSETTE INTERFACE

DOCUMENTATION UPDATE

AUGUST 1975

©MITS, Inc., 1975

PRINTED IN U.S.A.

MITS
"Creative Electronics"

P.O. BOX 8636
ALBUQUERQUE, NEW MEXICO 87108

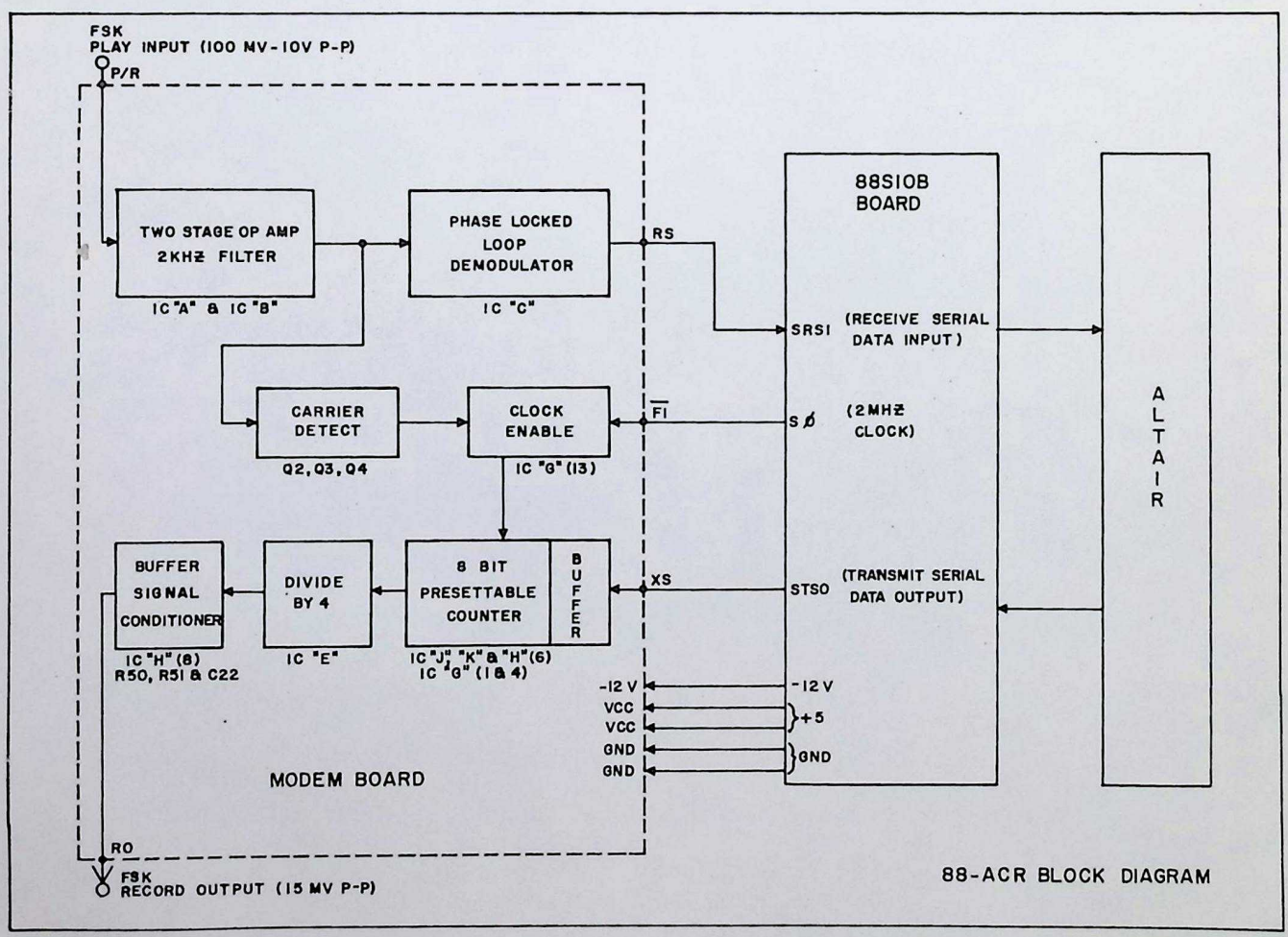
Theory of Operation

88-ACR OPERATION

The 88-ACR consists of an 88-SIO B, Serial TTL level I/O board, with a Modem board mated to it.

The Theory of Operation for the SIO B board is contained in its own documentation section within this manual.

Use the block diagram below for reference while reading the Theory of Operation for the Modem (Modulator-Demodulator) board which follows.



Modulator Operation

When an output program is running, serial data is being outputted on the "STSO" line from the 88-SIO B board. The changing logic levels are presented to the presettable counters, IC's J & K.

The counters (J & K) divide the 2MHz clock by 225 for a logic 1 input, and by 247 for a logic 0 input from the SIO B board. The output of IC K is further divided, by 4, using IC E. The resulting frequencies are 2225 Hz for a logic 1 input, and 2025 Hz for a logic 0 input from the SIO B board.

These signals are fed to the "Buffer Signal Conditioner". Here they are changed from TTL logic level square waves to 10mv peak-to-peak sawtooth waves suitable for the "Mic" inputs of tape recorders.

From the signal conditioner the signal is fed through the SIO B board connector and the shielded cable to the "Tape Record Out" jack on the back of the ALTAIR.

NOTE: "STSO" is normally a logic 1 with no data being trans transferred.

Demodulator Operation

When playing a tape to load data, the output of the tape recorder is fed into the miniature phone jack labeled "Tape Play In" on the back of the ALTAIR. At this point the audio levels should be between 35mv RMS to 3.5v RMS for proper operation.

This signal is fed by shielded cable through the connector on the SIO B board to the "P/R" connection on the Modem board. The signal is then filtered by IC's A & B and fed into the demodulator, IC C. The output of IC B is also fed to a carrier detector circuit (Q2, Q3 & Q4) that enables IC C and disables the 2MHz clock going to the modulator circuit.

IC C is a Phase Locked Loop which compares the frequency of the incoming signal with the frequency of its internal oscillator, which is set halfway between 2025 and 2225 Hz. The output of IC C is a corresponding logic 1 for 2225 Hz, or a logic 0 for 2025 Hz on its input.

A zener diode interfaces the output of IC C to TTL logic levels, which are then fed from "RS" on the Modem board to "SRSI" on the SIO B board.

USING THE 88-ACR

The 88-ACR Audio-Cassette Record Interface is designed to be used with any medium quality or better cassette tape recorder. Music quality recorders generally give better performance than smaller portable recorders.

If a stereo recorder is used, you may record on one track at a time. This will double the storage capacity, but prevent playback on any momaural machine.

Keep the recorder away from power transformers, flourescent lamps and other sources of electrical noise when recording or playing back tapes. For maximum performance, use low-noise tape when making all recordings.

Be sure that only the "Play In" or the "Record Out" of the 88-ACR is connected at any one time; never both.

Making a Recording From the 88-ACR

After a program has been loaded into the computer, connect "RECORD OUT" of the 88-ACR to the "Mic" of the recorder.

With the computer in a stopped condition, place the recorder into the record mode. Allow the recorder to run for at least 10 seconds, to allow for sufficient leader, before hitting the "RUN" switch on the computer. If you have a tape counter, start recording at "000" and hit the "RUN" switch at "015" to start recording data. Make note of the start and stop count of the data recorded.

If possible, it may be helpful to monitor the recording by listening with an earphone. This will give you a general indication if the 88-ACR and your program are functioning properly, and the data is actually reaching the recorder.

Most recorders use automatic level record circuits that need no adjustment of volume or tone settings during recording. If your recorder requires setting the record level, use 0 db or maximum undistorted level for recording.

Use this procedure for recording any data on cassette tape.

Loading Data From Tape with the 88-ACR

Before data may be loaded into the computer from a cassette tape, an input program of some type (e.g. Input Test Program) must first be loaded.

Once the input program is loaded, connect "PLAY IN" of the 88-ACR to the "Speaker", "Earphone" or "Line Out" output of your recorder. The volume and tone controls should be at their maximum settings.

Start playing the tape at the beginning of the leader ("000" if you have a tape counter); then hit the "RUN" switch on the computer before the data starts.

When the data input is complete, as indicated by the tape counter or halting of the input program, the recorder may be stopped.

This procedure should be used any time data is to be loaded from a cassette tape.

OUTPUT TEST PROGRAM

The following is a listing of the output program used to write test data onto tape. This will be used for the alignment of the 88-ACR Demodulator. The program may be used with any memory size, 256 words or larger.

This program will record the test byte (125) until the program is manually stopped. The program is written using I/O address 0 for status and I/O address 1 for data. If your board address has been wired differently, change the program accordingly.

ADDRESS LOCATION (octal)	OCTAL CODE	MNEMONIC	DESCRIPTION
200	333	IN	Input
201	000	---	I/O Port Status Address
202	346	ANI	And immediate with A
203	002	---	Anded data--mask for transmit buffer empty
204	312	JZ	Jump on zero
205	200	---	Lo
206	000	---	Hi — Address jumped to if zero accumulator
207	076	MVI	Move immediate to A
210	125	---	TEST BYTE
211	323	OUT	Output
212	001	---	I/O Port Data Address
213	303	JMP	Jump unconditional
214	200	---	Lo
215	000	---	Hi — Starting address of routine

INPUT TEST PROGRAM

The following is a listing of the program for playback of the Output Test Program. This program will also be used for the alignment of the 88-ACR Demodulator. It is written using the same I/O port addresses as the other program stated above, and should be changed accordingly if necessary.

ADDRESS LOCATION (octal)	OCTAL CODE	MNEMONIC	DESCRIPTION
000	333	IN	Input
001	000	---	I/O Port Status Address
002	346	ANI	And immediate with A
003	040	---	Anded data--mask for recieve data available
004	312	JZ	Jump on zero
005	000	---	Lo
006	000	---	Hi — Address jumped to if zero accumulator
007	333	IN	Input
010	001	---	I/O Port Data Address
011	356	XRI	Exclusive Or immediate with A
012	125	---	Exclusive Or Test Word
013	312	JZ	Jump on zero
014	300	---	Lo
015	000	---	Hi — Address jumped to if zero accumulator (Hi Addr. Test Prog.)
016	303	JMP	Jump unconditional
017	000	---	Lo
020	000	---	Hi — Address jumped to if zero accumulator

(cont.)

(cont.)

ADDRESS LOCATION (octal)	OCTAL CODE	MNEMONIC	DESCRIPTION
300	257	XRA	Exclusive Or register with A
301	062	STA	Store A direct
302	376	---	Lo
303	000	---	Hi — First address to be zeroed out
304	062	STA	Store A direct
305	377	---	Lo
306	000	---	Hi — Second address to be zeroed out
307	072	LDA	Load A direct
310	376	---	Lo
311	000	---	Hi — Address of data for above
312	306	ADI	Add immediate to A
313	001	---	Data to be added
314	062	STA	Store A direct
315	376	---	Lo
316	000	---	Hi — Address for above to be stored
317	322	JNC	Jump on no carry
320	337	---	Lo
321	000	---	Hi — Address to be jumped to for above
322	072	LDA	Load A direct
323	377	---	Lo
324	000	---	Hi — Address of data for above

(cont.)

(cont.)

ADDRESS LOCATION (octal)	OCTAL CODE	MNEMONIC	DESCRIPTION
325	306	ADI	Add immediate to A
326	001	---	Data to be added
327	062	STA	Store A direct
330	377	---	Lo — Address for above to be stored
331	000	---	Hi — Address for above to be stored
332	356	XRI	Exclusive Or immediate with A
333	006	---	Data to be Ex-Ored
334	312	JZ	Jump on zero
335	000	---	Lo — Address jumped to if zero accumulator
336	000	---	Hi — Address jumped to if zero accumulator
337	333	IN	Input
340	000	---	I/O Port Status Address
341	346	ANI	And immediate with A
342	040	---	Anded data--mask for recieve data available
343	312	JZ	Jump on zero
344	307	---	Lo — Address jumped to if zero accumulator
345	000	---	Hi — Address jumped to if zero accumulator
346	333	IN	Input
347	001	---	I/O Port Data Address
350	356	XRI	Exclusive Or immediate with A

(cont.)

(cont.)

ADDRESS LOCATION (octal)	OCTAL CODE	MNEMONIC	DESCRIPTION
351	125	---	Data to be Ex-Ored (Test Byte)
352	312	JZ	Jump on zero
353	300	---	Lo — Address jumped to if zero accumulator
354	000	---	Hi — Address jumped to if zero accumulator
355	303	JMP	Jump unconditional
356	000	---	Lo — Jump to this address if A is not zero
357	000	---	Hi — Jump to this address if A is not zero

MODEM BOARD VOLTAGE & WAVEFORM TEST DATA

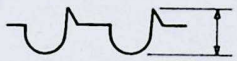
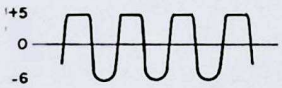
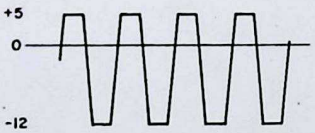
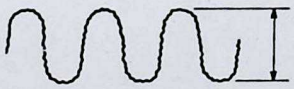
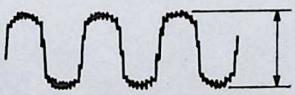
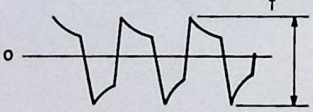
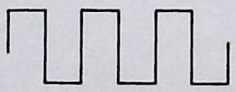
NOTE: All signals and voltages are measured with respect to ground.

The voltage measurements were taken with a 20K ohms/V VOM.

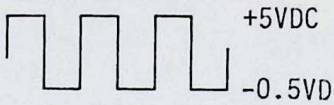
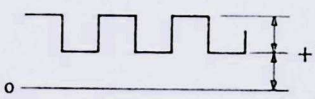
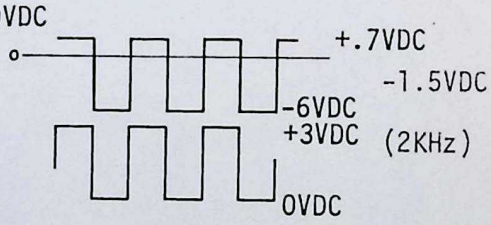
The voltage measurements may vary ±10%.

DEMODULATOR SECTION

Measurements on the following test points are given for both no input, and with a 1.5V P-P signal from a tape using the "Output Test Program".

TEST POINT		NO SIGNAL IN	1.5V P-P SIGNAL IN	
IC A uA741 FILTER	Invert. Inpt. Pin 2	OVDC		0.15V P-P
	Non-Invert. Inpt. Pin 3	OVDC	OVDC	
	Output Pin 6	OVDC (may be ±.1V)		(2KHz)
IC B uA741 FILTER	Invert. Inpt. Pin 2	OVDC		2V P-P (2KHz)
	Non-Invert. Inpt. Pin 3	OVDC	OVDC	
	Output Pin 6	OVDC (may be ±.1V)		(2KHz)
IC C XR-210 (P.L.L.)	Volt. Comp. In Pin 1	OVDC		1.2V P-P +1VDC
	Phase Det. Out Pin 2	-4VDC		2.5V P-P +1VDC
	Phase Det. Out Pin 3	-6.25VDC		.1V P-P +1.1VDC
	Phase Det. In Pin 4	-5.5VDC		2V P-P (2KHz)
	Phase Det. Bias Pin 5	-5.5VDC	OVDC	
	Phase Det. In Pin 6	-5.0VDC		1.4V P-P OVDC
	V- Pin 7	-12VDC	-12VDC	

(cont.)

TEST POINT		NO SIGNAL IN	1.5V P-P SIGNAL IN
Logic Output Pin 8 (cathode Z1)		+5VDC	 (Demodulated data)
VCO Fine Tune Pin 9		-11.5VDC	-11.5VDC
VCO Keying Inpt. (not used) Pin 10		-4VDC	-4VDC
VCO Gain & Sweep Cntrl.			
	Pin 11	-7VDC	-0.25VDC
	Pin 12	-6VDC	-0.5VDC
VCO Timing Capacitor	Pin 13	+3VDC	+3VDC
	Pin 14	+3VDC	+3VDC
VCO Output Pin 15			 2.5V P-P +2.5VDC (2KHz)
V+ Pin 16		+5VDC	+5VDC
Q2 (PNP Silicon EN2907)	E	+5VDC	+5VDC
	B	Open	+4.3VDC
	C	-7VDC	+4.3VDC
Q3 (PNP Silicon EN2907)	E	Open	+4.3VDC
	B	+5VDC	+3.6VDC
	C	-7VDC	+4.3VDC
Q4 (NPN Silicon CS4410/4437)	E	OVDC	OVDC
	B	OVDC	 (2KHz)
	C	+3VDC	

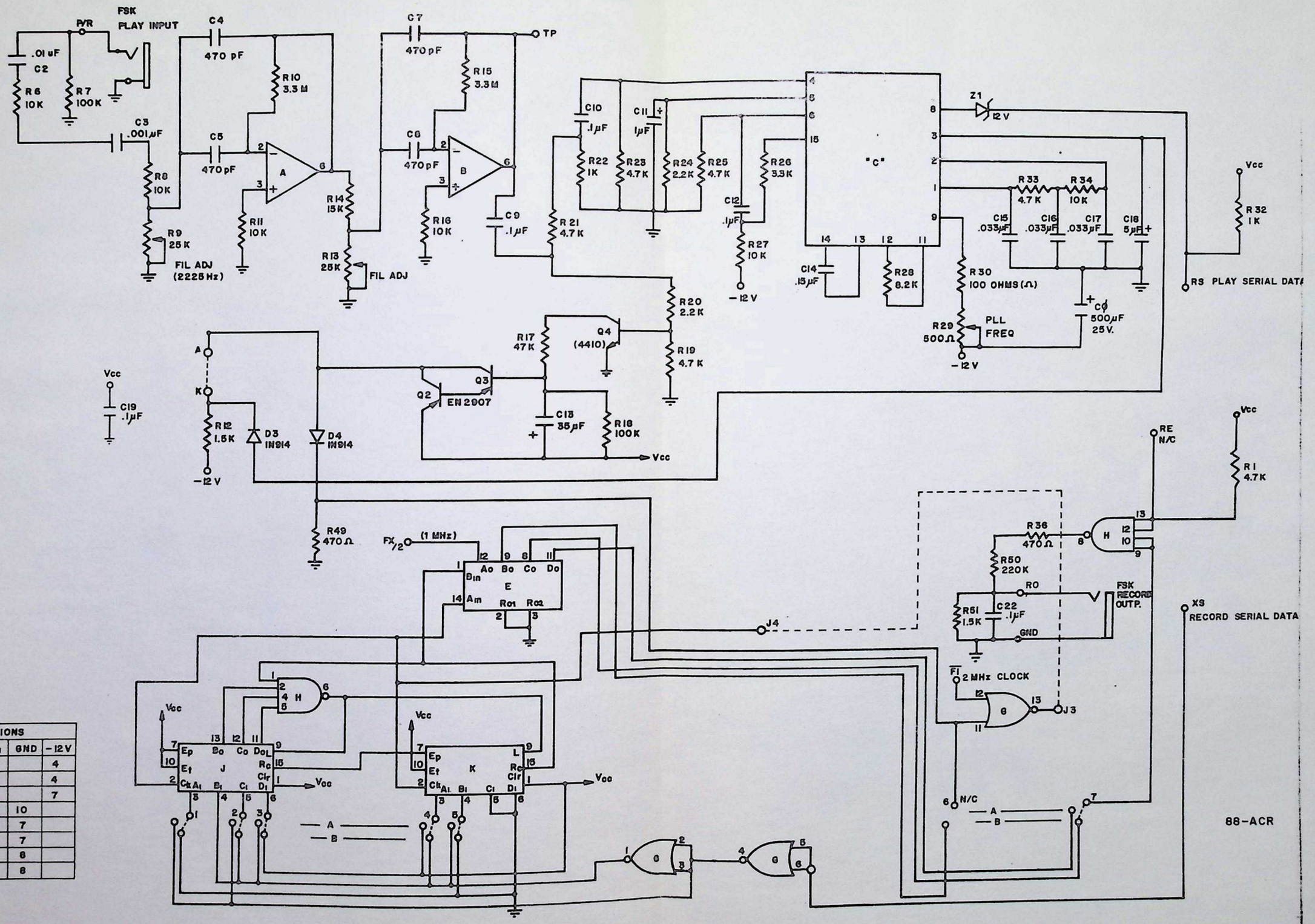
MODULATOR SECTION

Tests are made with no signal on the demodulator input. TTL logic voltage levels are used; logic 0 = -0.5v to +0.8v, logic 1 = +2v to +5.5v. The frequencies are within ±.05% of the values listed.

TEST POINT		MODULATOR INPUT XS = LOGIC 1	MODULATOR INPUT XS = LOGIC 0
IC E	Pin 1 ("B" ff input)	8900Hz-8us +pulse	8100Hz-8us +pulse
7493	Pin 9 ("B" ff out)	4450Hz-sq. wave	4050Hz-sq. wave
4-bit ctr.	Pin 8 ("C" ff out)	2225Hz-sq. wave	2025Hz-sq. wave

(cont.)

TEST POINT		MODULATOR INPUT XS = LOGIC 1	MODULATOR INPUT XS = LOGIC 0
IC G	Pin 1 Output	Logic 1	Logic 0
7402	Pins 2 & 3/4 Inpt./Out.	Logic 0	Logic 1
Quad 2-Inpt.	Pins 5 & 6 Input	Logic 1	Logic 0
NOR	Pin 11 Input	+.5VDC (goes to +3.5VDC with signal to the demodulator to inhibit pin 13)	
	Pin 12 Input	2MHz sq. wave	2MHz sq. wave
	Pin 13 Output	2MHz sq. wave	2MHz sq. wave
IC H	Pin 1 Input	8900Hz-8us +pulse	8100Hz-8us +pulse
7420	Pin 2 Input	500KHz-sq. wave	500KHz-sq. wave
Dual Quad	Pin 4 Input	250KHz-sq. wave	250KHz-sq. wave
Inpt. NAND	Pin 5 Input	125KHz-sq. wave	125KHz-sq. wave
	Pin 6 Output	2225Hz-500ns -pulse	2025Hz-500ns -pulse
	Pin 13 Input	+5VDC	+5VDC
	Pin 12 Input	+5VDC	+5VDC
	Pin 10 Input	2225Hz-sq. wave	2225Hz-sq. wave
	Pin 9 Input	2225Hz-sq. wave	2225Hz-sq. wave
	Pin 8 Output	2225Hz-sq. wave	2225Hz-sq. wave
IC J	Pin 2 Clock Inpt.	2MHz	2MHz
9316/74161 Presettable 4-bit ctr.	Pin 15 Ripple Carry Out.	125KHz-500ns +pulse	125KHz-500ns +pulse
IC K	Pin 2 Clock Inpt.	2MHz	2MHz
9316/74161 Presettable 4-bit ctr.	Pin 15 Ripple Carry Out.	8900Hz-8us +pulse	8100Hz-8us +pulse



POWER CONNECTIONS				
IC	TYPE	V_{CC1}	GND	-12V
A	741	7		4
B	741	7		4
C	XR 210	16		7
E	7493	5	10	
G	7402	14	7	
H	7420	14	7	
J	9316	16	8	
K	9316	16	8	